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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/820,580	04/08/2004	Stephen L. Morein	00100.02.0003	8567

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EXAMINER	
SINGH, DALIP K	
ART UNIT	**PAPER NUMBER**
2671	

DATE MAILED: 12/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/820,580	MOREIN ET AL.	
	Examiner	Art Unit	
	Dalip K. Singh	2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 4 recites the limitation "the controller" in claim 4, line 1. There is insufficient antecedent basis for this limitation in the claim.

2. Claim 6 is objected to because of the following informalities: claim 6 at line 2 recites "...a level on...", it should be a level one. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 2, 3 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by US 6,889,291 B1 to Palanca et al.

a. Regarding claim 1, Palanca et al. **discloses** a main memory (main memory 160, Fig. 1); a level one cache (L1 cache 120, Fig. 1), coupled (...multi-processor device 110 is connected to bus 170...col. 4, lines 24-35) to the main memory (main memory 160), for maintaining information (...memory devices 160 are used by the processors in device 110 to carry out program instructions...col. 4, lines 30-35); and a level two cache (L2 cache 130, Fig. 1), coupled between the main memory (main memory 160) and the level one cache (L1 cache 120)(...L2 cache 130 acts as an intermediary between main memory 160 and L1 cache 120...col. 4, lines 36-41).

b. Regarding claim 2, Palanca et al. **discloses** a graphics controller (graphics processor 113, Fig. 1) operative to send requests to the main memory (...when data

sought by CPU 111 or graphics processor 113 is not already in the L2 cache 130 or L1 cache...needs to be extracted from main memory 160...col. 8, lines 39-47).

c. Regarding claims 3 and 5, Palanca et al. **discloses** a cache having many blocks which individually store the various instructions and data values (...A cache has many "blocks" which individually store the various instructions and data values. The blocks in any cache are divided into groups of blocks called "sets"...col. 1, lines 19-37). Palance et al. **further discloses** multi-level caches which are interconnected (...Although Fig. 1 depicts only a two-level cache hierarchy, multi-level cache hierarchies can be provided where there are many levels of interconnected caches...col. 4, lines 13-23).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 4 and 6-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,889,291 B1 to Palanca et al. as applied to claim 1 above above, and further in view of US 6,195,106 B1 to Deering et al.

a. Regarding claim 4, Palanca et al. **is silent about** graphics controller sending requests to plurality of cache blocks, and the level two cache storing those requests being sent to the plurality of cache blocks. Deering et al. **discloses** a graphics controller (rendering controller 70, Fig. 1) sending writes to each L1 cache block which are subsequently transferred to the memory (DRAM banks A-D) through a level two (L2) pixel cache, thereby storage of such requests at level two (L2) pixel cache is disclosed. Therefore, it would have been obvious to a person of ordinary skill in the art at the time

invention was made to modify the Palanca et al. with the feature "storing graphics controller requests to level one cache being stored in level two cache" as taught by Deering et al. **because** this avoids having to access the main memory unless absolutely required (if level two cache does not have the requested data) and thus miss costs are minimized resulting in improved graphics operations (col. 10, lines 34-60).

b. Regarding claim 6, it is similar in scope to claims 4 and 5 above and is rejected under the same rationale.

c. Regarding claim 7, Palanca et al. **discloses** a main memory (main memory 160) coupled to the level two cache ((L2 cache 130, Fig. 1). Palanca et al. **discloses** a cache having many blocks which individually store the various instructions and data values (...A cache has many "blocks" which individually store the various instructions and data values. The blocks in any cache are divided into groups of blocks called "sets"...col. 1, lines 19-37). Palance et al. **further discloses** multi-level caches which are interconnected (...Although Fig. 1 depicts only a two-level cache hierarchy, multi-level cache hierarchies can be provided where there are many levels of interconnected caches...col. 4, lines 13-23).

d. Regarding claim 8, Palanca et al. **discloses** main memory (main memory 160) being coupled to a graphics controller ((graphics processor 113, Fig. 1). Palanca et al. further **discloses** cache 400 (Fig. 4A-4D) wherein at a cache miss occurrence when data is being sought by the graphics controller is not already in the L2 cache, 130 or L1 cache 120 and has to be fetched from main memory 160 and the update mechanism maintains coherency of data by placing it in L2 cache, 130 (...a cache miss occurs when data sought by CPU 111 or graphics processor 113 is not already in the L2 cache, 130 or L1 cache 120 but needs to be extracted from main memory 160. Once extracted from main memory

160, the update mechanism determines coherence to place the data within cache 130...col. 8, lines 35-47).

e. Regarding claims 9, 10 and 11, they are similar in scope to claim 8 above and are rejected under the same rationale.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Dalip K. Singh** whose telephone number is **(571) 272-7792**. The examiner can normally be reached on Mon-Friday (10:30AM-6: 30PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Ulka Chauhan**, can be reached at **(571) 272-7782**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, please contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). Please note that the new Central Official FAX number for application specific communications with the USPTO is **571-273-8300** (effective July 15, 2005).

Dalip K. Singh
Examiner, Art Unit 2671

dks
December 22, 2005

ULKA CHAUHAN
SUPERVISORY PATENT EXAMINER